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# FPGA based Fast Integrated Real-Time Multi Coincidence Counter Using a Time-to-Digital Converter

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**Abstract**—The precise measurement of time is very important in many engineering and science applications. In some of the applications the time measurement is used to investigate the correlation between the timing of events and coincidence counters are employed for this purpose. Coincidence counters are commonly used as instruments in applications such as gamma ray correlation in positron emission tomography(PET) and gating events of interest from background noise in quantum physics experiments. In order to implement coincidence counters, time-to-digital converters can be used. While providing precise measurement, it is also important to maintain real-time operation and fast data processing due to the change in interest of events during the application. In this research, we have developed a real time multi-coincidence counting scheme in a Field Programming Gate Array (FPGA) based on our 8-channel time-to-digital converter(TDC) which we have published. With this method we have managed to combine an 8 channel TDC with a coincidence counter in the same FPGA chip while providing real-time operation and high precision. The smallest coincidence window, our system can provide is 15 ps and at 150 ps our system is capable of detecting the maximum number of coincidences. Also, the functionality of the coincidence counter has been proved by tests of coincidence rate as a function of window size and coincidence rate as a function of delay.

**Keywords**--Time-to-Digital Converter, Coincidence Counting, Coincidence Detection, Avalanche Photo Diode, Positron Emission Tomography, Field Programming Gate Array.

## I. INTRODUCTION

Precise time measurement and correlation are essential in many science and engineering applications. Coincidence counters are utilized for measuring the correlation between simultaneous time events. They can be found in applications such as the measurement of the delay between Avalanche Photo Diodes(APD) in photonics, the identification of entangled particles from the background noise through correlation in quantum physics experiments and the tumor detection through the correlation of gamma ray emissions in Positron Emission Tomography(PET) scanners.

The phenomenon of coincidence occurs when two time events from different channels trigger in the same time interval [1]. This time interval is defined as the coincidence window  $T_w$ . The combination of event patterns from different channels forms the coincidence address and these addresses are counted as they are detected. For instance, in a PET scanner, simultaneous hits of gamma rays to the detectors is defined as a coincidence. An illustration of a coincidence and a coincidence address can be seen in figure 1.

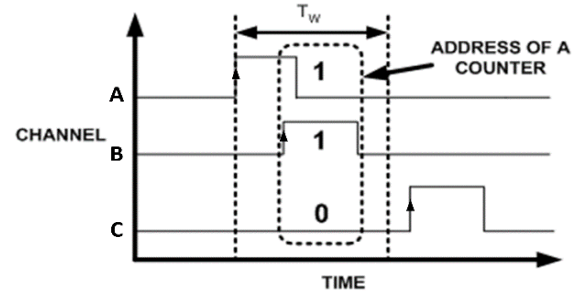


Figure 1: Illustration of AND gate based coincidence counter

The width of the coincidence window determines the precision of a coincidence counter and narrower windows are more precise. High precision is desired in areas such as medicine, nuclear science and quantum [2] [3] [4] .

The most basic coincidence counting implementation would be an AND gate which takes two or more inputs and outputs a logical high if all inputs are high. However, such scheme has a coincidence window limited to how fast the AND gate can produce a result. The Ortec Co4020 Quad device is an example of this kind of implementation [5]. The illustration of an AND gate-based coincidence counter can be seen in figure 2,  $\Delta T$  represents the delay between input and the output of the gate.

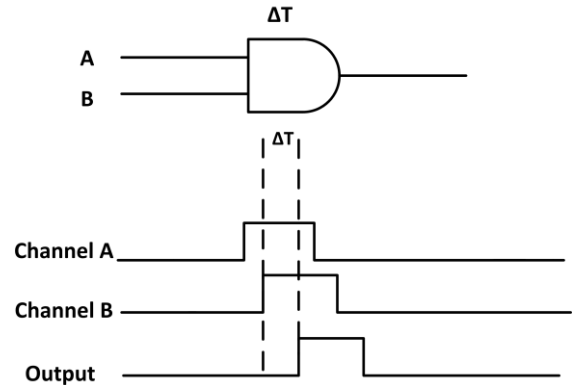


Figure 2 : Illustration of AND gate-based coincidence counter

To achieve narrower coincidence windows, time stamps of the trigger events could be used. This could be implemented through use of a TDC. There are several examples to TDC based coincidence counters such as [6] where an external TDC board and external 'AND' logic have been used. Very similar implementation is also described in [7].

A time-to-digital converter (TDC) is an instrument used to generate time stamps for the events happening in the time domain. The simplest TDC consists of a coarse counter, which starts counting with the START signal and counts until the STOP signal is detected. The counter value at STOP represents the digitalized value of the time interval between START and STOP. However, the coarse counter method will not be able to detect events shorter than the clock period. To measure intervals shorter than the clock period, fine time TDCs are needed.

Asynchronous logic elements located in FPGA chips, such as carry chains, can be used to implement fine time TDCs. Since carry chains are asynchronous from the clock, they can be used to divide the clock period into shorter time intervals. In many implementations pico-second range resolutions have been achieved by using fine time TDCs, see [8] [9] [10].

In a typical FPGA based TDC, time intervals shorter than the clock period are measured by carry chain-based delay lines and this measurement is called the fine time interpolation. However, time intervals greater than the clock period are still measured by the coarse counter since it would not be space efficient to use carry chains for time intervals far greater than the clock period. The combination of fine and coarse interpolation is called hybrid interpolation [11]. An illustration of such scheme can be seen in figure 3.

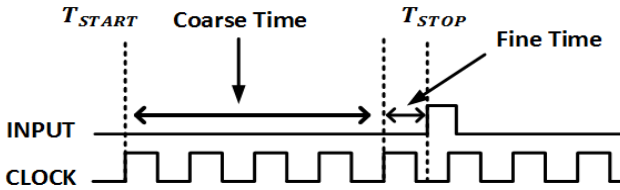


Figure 3 : Illustration of a hybrid interpolation

In a typical fine time TDC, a carry chain produces a thermometer code for the relative position of the trigger signal to the next clock edge. The thermometer code is converted to an n-bit fine code by a priority encoder to form a fine time code.

In this research, we have developed a multi-channel coincidence counting scheme based on our multi-channel TDC scheme that we previously published [11]. This scheme provides integration of both coincidence counting and time tag generation into the same FPGA fabric to provide fast real-time computation. In this research, implemented coincidence counting logic avoids buffering of any tags like histogram-based methods [12]. Thus, dropping tags in the case of heavy input traffic has been prevented.

## II. THE SYSTEM ARCHITECTURE

As it described in [7][12] previously, TDCs are used for coincidence detection. However, our proposed architecture differs from them by providing real-time coincidence detection and counting while sharing the same FPGA fabric with the TDC. This avoids any buffering required between components which could result in data loss under heavy channel traffic. In this implementation we have used Xilinx Spartan 6 LX150 FPGA. When 8-channel TDC and coincidence counter has been synthesized the total of 5,846 slices out of 23,038 slices so, roughly 25% of the available slices have been used. This indicates potentially, further improvement in channel number could be possible in the future.

Our architecture consists of two blocks, which are a TDC block and a coincidence counting block. In this section the details of these blocks will be discussed.

### A. Time-to-Digital Converter

As described in [13], our TDC is a 512-staged carry chain-based delay line which we have implemented by using CARRY4 primitives in Xilinx Spartan 6 LX150 FPGA. We have used an Opal Kelly XEM6310 board in this research. Our TDC is based on a hybrid time interpolation method which combines coarse and fine time measurements. In this implementation, the system clock runs at 125 MHz. Thus, the coarse counter increments every 8 ns. The average time resolution achieved by our TDC is 21 ps and the least significant bit (LSB) resolution was set to 15 ps. This means a single bit in our time stamps represents a 15 ps. In addition, our TDC can support up to 8 channels and it has 8 ns dead time on each channel.

Some alterations have been done on our tag format since the publication of the our TDC scheme. Currently the tags generated by TDC consisted of 19 bits of coarse and 9 bits fine and 4 bits of channel identification tag.

A diagram of our TDC scheme can be seen in figure 4.

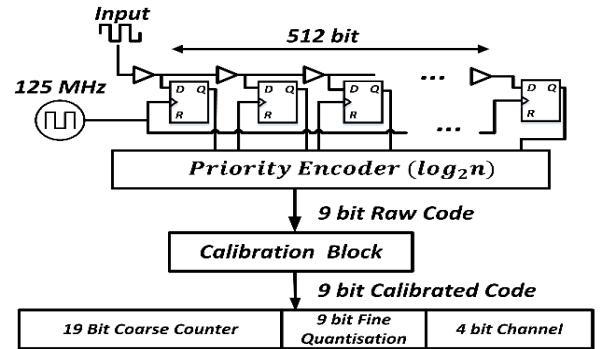


Figure 4 : Illustration of time to digital converter scheme

The one common problem among the FPGA based delay line TDCs is non-equal bin sizes throughout the delay line. This is mainly caused by the FPGA routing and the temperature change during the operations and this leads to non-linearity in delay elements. To fix this issue, a calibration scheme is required.

As it was discussed in [8], we have also implemented on-the-fly calibration for our TDC within the FPGA fabric. The calibration is based on the code density calibration method which was described in [8]. The calibration of TDC provides a transfer function which is stored in a look-up table and used whenever a new tag is generated by the TDC.

Currently, the main limitation of our implementation is having a dead time limited to the clock period which is 8 ns. Therefore, it cannot process events that are generated at periods shorter than 8ns. Also having a greater dead-time increases the error rate in the operation since greater intervals are more likely to have uncorrelated triggers such as randomly occurring dark counts or any other noise within the same 8 ns window with valid triggers.

### B. Coincidence Counter

The TDC block has been designed to calculate the delta time between tags from one reference channel and tags from the other channels continuously. This property is used to implement a coincidence counter. The coincidence counter essentially checks the difference between two tags and decides whether the difference is

within the coincidence window  $T_w$ . Since TDC modules gives out a delta time between  $T_{start}$  and  $T_{stop}$  continuously, the coincidence detection can be placed just after this operation.

Coincidence detection gets activated as the tag correlator outputs a tag. According to time differences between tags the coincidence addresses are formed. The formed coincidence addresses are used as an index of the memory location in the RAM block and when a new address is detected the corresponding address gets incremented. Once in every 600 ms, the content of this RAM sends out through the FIFO. After the data is sent out, the system restarts and the RAM block gets cleared up. The sent data is displayed on the PC screen by the software interface. The block diagram of coincidence counting scheme is shown in figure 5.

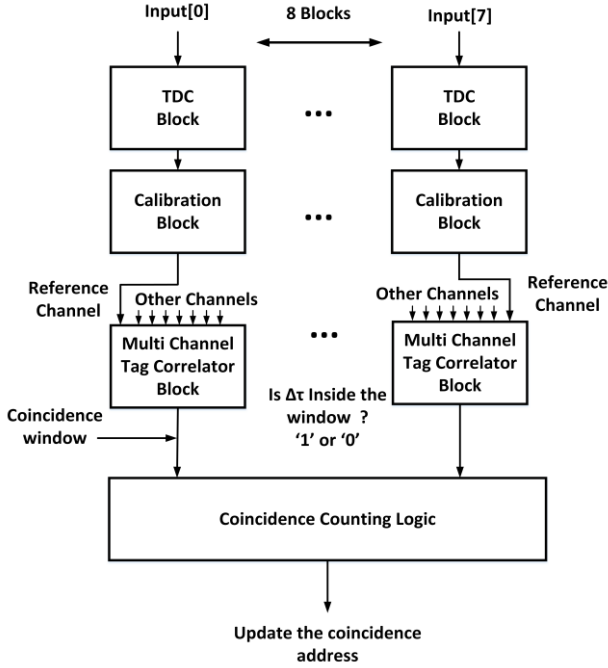


Figure 5 : Illustration of a coincidence counting scheme

The software interface can vary the coincidence window according to a need. The smallest possible value "1" corresponds to 15ps since the LSB is 15ps so, the smallest coincidence window that the system can input is 15 ps.

In addition, adding a digital delay on each channel is possible through the software. Since the TDC generates time stamps, adding n number delay corresponds to delaying the channel n times 15 ps. This is a useful feature and one of the advantages of using TDC based coincidence counters. Thus, the delay between two channels can be measured by simply by delaying one channel until it becomes correlated with the other channel, without adding any physical delay into the system. This property is very useful in applications where the delay between two detectors has been investigated.

### III. RESULTS

By using the implementation scheme discussed in section II, a TDC based real time coincidence counter has been successfully implemented in a FPGA. In order show the working coincidence counter, some tests have been conducted on our system. These tests were the observation the coincidence rates a function of delay and coincidence rate as a function of a window size. For the tests,Thurlby

Thandar Instruments TGP110 10MHz pulse generators have been used.

#### A. Coincidence Rate as Function of Delay

The coincidence rate as a function of delay test simulates, delay measurement between 2 channels. In this test two signal generators, which are in sync with each other, have been used. The delay between signals generators has been set to a fixed value of approximately 75 ns. The signal generators' frequency was 1.13 MHz (880ns) during this test. Thus, from 600 ms / 880 ns approximately 680,000 tags were generated Also window size was set to certain value and kept constant throughout the test. This test expecting an increase and saturation of coincidence rates as the difference between two channels' times stamps reduces.

Every 600 ms, digital delay has been introduced to lagging channel and the change in double fold coincidence rate between channels has been observed. Firstly, we tested our design with narrow windows sizes such as 15ps, 30 ps, 45 ps, 75 ps, 105 ps, 150 ps and 300 ps and a 15 ps delay was added every 600 ms. A graph of coincidence rate as a function of delay for narrow window sizes can be seen in figure 6.

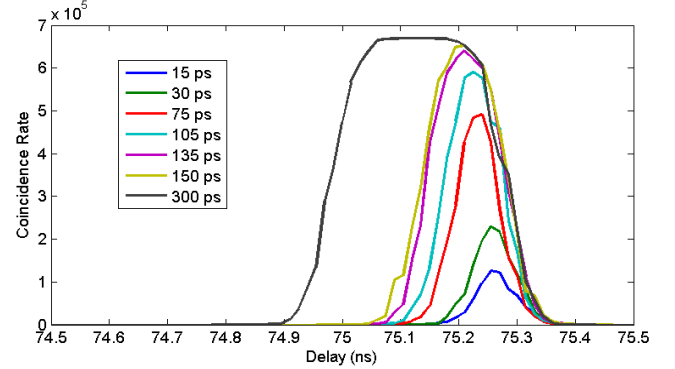


Figure 6 : The coincidence rate as function of delay

As it was shown in figure 6, as the window narrows the coincidence rate drops. With the 150 ps window, the highest coincidence rate was observed, and the highest rate stayed the same as the window sizes were widened. Also, this graph shows the coincidence rates of all different window sizes intersects at around 75.3ns which indicates the delay between the two channels. Thus, it proves the functionality of measuring the delay between the two channels accurately.

We have also tested wide window sizes such as 4.95ns, 7.5 ns, 15 ns and 30 ns, a 15 ps delay added every 600 ms. The change in coincidence rate can be seen in figure 7.

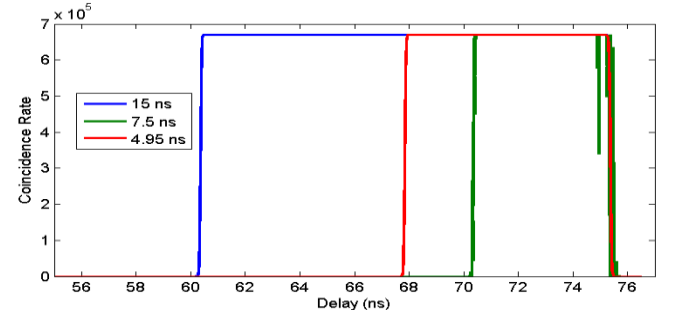


Figure 7 : Coincidence count as function of delay

### B. Coincidence Rate as a Function of Window Size

The coincidence rate as a function of window size is a test conducted to show how the change in coincidence window affects coincidence rates. This test expects an increase in coincidence rates as the window size increases and saturation after a certain threshold which corresponds to the delay between channels. To conduct this experiment, a setup same as the first test was used. The delay is kept constant between tags in this test. However, the windows size varies. The delay between channels was set to approximately 75 ns and the each 600 ms the windows size is expanded by 15 ps. Also, the input signals were again 1.13 MHz (880ns) so, approximately 680,000 tags were generated.

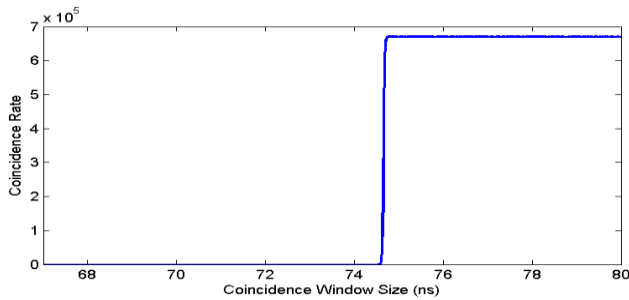


Figure 8 : Coincidence rate as function of window size

As a result, of this test we have observed the saturation around 75 ns window size which was expected before the experiment since the delay between the channels was approximately 75 ns. The graph of coincidence rate as a function of window size can be seen in figure 8.

### IV. CONCLUSION

In conclusion, coincidence counters are correlation tools used to detect simultaneously happening time events over multiple channels. They can be found in many different science and engineering applications.

We have developed a coincidence counting scheme based on the previous work we have done on TDCs for Lidar correlation [8]. Our TDC method is used to correlate the events happening in different channels and we have used this property to implement a fast and real-time coincidence counting scheme. This research aims to provide an useful instrument that can be potentially integrated into medical imaging systems or quantum physics experiments where the correlation between events are investigated, i.e PET scanners, APD calibration, quantum physics experiments etc. Our design is unique in a way that merges all the coincidence counting and time stamp generation logic into the same FPGA fabric. This provides fast precise real time operation without losing any data through inter-devices data transfer protocols.

For this implementation we have used Spartan 6 LX150 FPGA which was located on an Opal Kelly XEM6310 board. Our TDC has 21 ps average resolution where the least significant bit of our TDC was set to 15 ps. Thus, the smallest window that can be set is 15 ps.

Also, coincidence rate as function of delay and coincidence rate as function of window size tests have been conducted. Our tests showed, coincidence windows size below 150 ps seemed to be missing some of the tags. So ideally window sizes greater than 150 ps seems to yield to better results.

In the future, our system will be tested with more than 2 channels since it supports up to 8 channel time tagging. In addition, it is planned to work on reducing the 8 ns dead time and improving the 21 ps average resolution to sub 15 ps. For this reason, alternatives to carry chains have been being researched. Improving the resolution will result potentially increase in coincidence rates being detected with narrower coincidence window sizes. Also, testing the system in an actual quantum physics experiment and integrating it into different applications is a part of the future work.

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